Module Title	Digital Logic Design
Course Title	BEng (Hons) Electrical and Electronic Engineering/Electrical Power Engineering/Electronic and Computer Systems Engineering
School	☐ ASC ☐ ACI ☐ BEA ☐ BUS ☒ ENG ☐ HSC ☐ LSS
Division	BEng Electrical and Electronic Engineering/Electrical Power Engineering/Electronic and Computer Engineering
Parent Course (if applicable)	
Level	Level 4
Module Code *(showing level)*	EEE_4_DLD
JACS Code (completed by the QA)	
Credit Value	20 credit points
Student Study Hours	Contact hours: 50, 12 hours recorded online material (FT and PT) Student managed learning hours: 150 Placement hours:
Pre-requisite Learning	None
Co-requisites	None
Excluded combinations	None
Module co-ordinator	TBC
Short Description (max. 100 words)	The module covers the fundamental theory for the design of and the practical uses of digital electronics in the two design domains of combinational logic design and sequential logic design. The process of developing digital logic design is modelled using Hardware Description Languages (HDL). The module studies hardware devices to build circuits for digital logic designs and tools to support the design and analysis of those circuits; these include standard logic gates and Field Programmable Gate Arrays (FPGA). The module covers common design blocks such as adders, encoders, comparators, data selectors, flip-flops, counters, registers. The module shows the design and implementation of full digital systems typically based around finite state machines from description in HDL to implementation using FPGA technology.

Aims	Learn and develop the theory and methodologies of combinational and sequential digital logic so that students gain the ability to analyse their operation as well as be able to design basic combinational and sequential circuits Learn and develop the ability to describe combinational and sequential logic designs using Hardware Description Languages Develop practical skills for students to employ lab equipment to build and test digital circuits Develop knowledge and skills to employ standard workshop instruments for monitoring the operation of digital circuits Develop written communication skills (through digital notebooks) to analyse and compare laboratory experiments with annotations of the design, analysis and testing of digital circuits
Learning Outcomes (4 to 6 outcomes)	Knowledge and Understanding: • Explain and discuss the underlying principles and practices of the design of digital logic for the building of combinational and sequential circuits from Boolean equations, through logic minimisation up to analysis and synthesis of sequential designs (A1, A2) [AHEP3 SM1i] • Describe the modelling of digital logic design using Hardware Description Languages (A1, A3) [AHEP3 D4i, P4i] Intellectual Skills: • Understand the mapping of logic concepts to digital components such as gates, latches, flip-flops for building operational circuits (B1, B2) [AHEP3 EA3i] • Apply knowledge of Hardware Description Languages to model digital logic designs to build digital circuits in FPGA technology (B3, B4) [AHEP3 P2i, G1] Practical Skills: • Gain the ability to build circuits on breadboard from schematics and make them operational. Use commercial tools to create projects to deploy digital logic design in FPGA technology (C2, C3) [AHEP3 P3i] • Develop fault-find abilities of digital circuits using logic probes and test instruments (C2, C7) [AHEP3 EA2i, P1i]
Employability	The module develops the understanding and application of Hardware Description Languages (HDLs) such as Verilog to model and design digital circuits which are essential skills in roles such as “Digital Design Engineer”, “Hardware Design Engineer” or “RTL Design Engineer” used widely in the industry. Companies such as ARM, Mobile phone manufacturers, GE, Phillips, Cirrus Logic continuously advertise these roles.
Teaching and learning pattern	Contact hours includes the following: (please click on the checkboxes as appropriate) √ Lectures ☐ Group Work: ☐ Seminars ☒ Tutorial: ☐Laboratory ☒ Workshops ☒ Practical ☒ VLE Activities

Indicative content	Number Systems and Conversions, Boolean Algebra and Logic Equations, Logic Minimisation, Combinational Logic Blocks, Flip-Flops, Registers, Finite State Machines. All this content is expressed in HDL and tested in FPGA devices.
Assessment method (Please give details – of components, weightings, sequence of components, final component)	Formative assessment: Short-training Moodle Quizzes, Online QAs, use of logic simulators. Summative assessment: CW: 50% (A1, A3, C2, C3, C7). Composed of two sub-components: SC1_50 and SC2_50 Exam: 2 hours exam 50% (A1, A2, A3, B1, B3). Overall, the assessment components are: CW_50 (SC1_50 + SC2_50) and EX_50
Mode of resit assessment (if applicable)	Formative assessment: Tutorials online Summative assessment: CW: 5 hour-long session in lab Exam: 2 hours exam (50%)
Indicative Sources *(Reading lists)*	Core materials: 1. Fundamentals of Logic Design: Enhanced Edition | 7th Edition; Charles H. Roth Jr., Larry Kinney and Eugene B. John. Cengage Learning, 2020. 2. Digital System Design with SystemVerilog; Mark Zwolinski. Prentice Hall, 2009 Optional reading: 1. FSM-based Digital Design using Verilog HDL; Peter Minns and Ian Elliot. Wiley 2008. 2. A Verilog HDL Synthesis: A Practical Primer; J. Bhasker. Star Galaxy Publishing, 1998
Other Learning Resources	VLE for this module, Quartus Software from Intel, IcarusVerilog, LogicFriday, Espresso, https://www.digitalelectronicsdeeds.com/; https://www.edaplayground.com/